L1: Entry 26 of 163 File: USPT Nov 27, 2001

DOCUMENT-IDENTIFIER: US 6324602 B1
TITLE: Advanced input/output interface for an integrated circuit device using two-level to multi-level signal conversion

Detailed Description Text (12):
The multi-level protocol signal output by each BCC 24 can be a synchronous signal which is output at a double data rate (DDR)--i.e., clocked on both the rising and falling edges of a clock signal. In one embodiment, each BCC 24 will compress multi-bit information in one clock cycle on a per-pin basis.

CLAIMS:

9. The advanced input/output interface of claim 1, wherein each of the bit compression circuit and the bit decompression circuit utilizes a double data rate technique.

14. The integrated circuit memory of claim 10, wherein each of the bit compression circuit and the bit decompression circuit utilizes a double data rate technique.